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Electromagnetic Modeling and Optimization of Packaged Photodetector Modules for 100 Gbit/s Applications

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Introduction

The optical-fiber communication system operating at 100 Gbit/s is recently considered to be an ideal candidate as the next generation communication system [1]. High speed photodetectors (PDs) with high efficiency are key components for 100 Gbit/s transceivers. InP-based PD chips exceeding 130 GHz bandwidth have been developed [2]. PD chips are packaged in modules for the purpose of system experiments. Figure 1 (a) shows the inside view of a packaged PD module. In the module, a conductor-backed coplanar waveguide (CBCPW) line is adopted to bridge from the PD chip to the 1mm coaxial connector [3]. The CBCPW line is connected to the chip with bonding wires, and the connector is conductively glued directly on it. Figure 1 (b) shows the relative frequency response of both the chip and the module, which is a normalized O/E conversion characteristic of the device. The bandwidth of the module decreases to be 80 GHz comparing with the one of the chip being about 110 GHz.

The degraded bandwidth, which is due to the packaging structure of the PD module, will have an impact on the bit-error rate (BER) in an optical transmission system. The packaging of these high-speed components is very challenging when aiming at the rate of 100 Gbit/s, especially due to the multi-chip module (MCM) structure involving several chip-to-chip and/or chip-to-substrate transitions. The transition from the CBCPW to the connector was previously investigated and optimized using electromagnetic (EM) simulations [4], [5]. In this paper, full 3D electromagnetic (EM) behavioral models of PD chips are firstly proposed for the EM simulations on chip-to-CBCPW wire-bonding transitions. Afterwards, bonding wires employed in transitions are systematically analyzed by EM simulations using Ansoft HFSS.

Full 3D Electromagnetic Behavioral Modeling of PD Chips

EM models of PD chips, which contain the relative frequency response of the PD chip, are necessary for identifying the source of bandwidth limitation in chip-to-CBCPW wire-bonding transitions by EM simulation. Although full 3D EM modeling usually refers to passive structures, this paper firstly demonstrates that active devices such as photodiodes can also be fully modelled in the 3D EM simulator.

Figure 2 (a) shows an EM model of the PD chip which resembles a typical on-wafer measurement setup. At the end of the chip, a taper shaped excitation structure models the ground-signal-ground probe in measurements. In order to obtain an accurate simulated characteristic of the chip model compared to the measured one, the parasitic elements of the excitation structure have to be removed by EM calibration [6]. The metallization layout of the chip is consistent with the real device including large block capacitors and air-bridge structures. Matching resistance is employed to improve the bandwidth of the chip. The bandwidth of the chip is affected by the parasitic elements on the chip, which are built in the EM model, and the embedded pin photodiode. The bandwidth of the photodiode is mainly

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limited by the capacitance of the diode and the transit-time effect. The insert in figure 2 (a) shows the equivalent circuit of the pin photodiode in the EM model. Due to the limitation of the EM simulator, only a capacitance is included in the model to capture the bandwidth limitation of the photodiode. The photocurrent source and the parallel inversed biased resistance of the photodiode are modeled by the lumped port with high internal impedance in the simulator. As shown in figure 2 (b), the relative response of the EM behavioral PD model perfectly fits the measured one.

Systematic Analysis on the Wire-bonding Transitions

The EM behavioral model is then used to analyze the impact of the bonding wire interconnect up to 130 GHz. An EM model of PD chip-to-CBCPW wire-bonding transitions is illustrated in figure 3 (a). Three bonding wires connect each pad of the chip to the signal (S) or ground (G) strips of the CBCPW, respectively. The transmission characteristic of wire-bonding transitions is considered to be influenced by the arrangement of bonding wires, the number of bonding wires in the transition, the length of the wires (l), the height of the wires (h), the horizontal level difference (d) and the gap (g) between the chip and the CBCPW. The parameter abbreviations are indicated in figure 3 (b). We have already shown previously that wire bonding can exhibit a similar performance compared to flip-chip technology even at frequencies in the millimeter-wave range.

Selected simulated relative responses of the wire-bonding transition are shown in figure 4. The attenuation of them becomes very serious beyond 60 GHz, which is similar to the measured one of the module. Therefore, wire-bonding transitions are identified be to the major bandwidth limitation of the PD module. Figure 4 (a) demonstrates that there should be an optimized gap between the chip and the CBCPW to avoid fast attenuation beyond 60 GHz and the deep notch around 90 GHz. Figure 4 (b) shows that more bonding wires result in better relative response. Figure 4 (c) and (d) show that bonding wires connecting ground traces should be placed close to the gap of CBCPWs and all wires should spread well along the width of strips. Following these guidelines the impact of the bonding wires can be diminished substantially.

Conclusion

In this paper, we propose an accurate full 3D EM behavioral model of PD chips for the first time. The model, which is meshed at 130 GHz, runs for about 17 minutes on an Intel Core2 Duo CPU@3GHz PC with 3.5GB of RAM. The impact of various parameters in wire-bonding transitions for transmission characteristic is summarized in the Table I. When numbers of bonding wires are placed separately all through strips of CBCPWs as well as keeping an optimized gap of transitions, more than 10 GHz bandwidth improvement can be achieved compared the worst case. We also notice that optimization on bonding wires does not significantly improve the fast decay beyond 60 GHz. Further investigation and optimization of the transition is required including a redesign of the CBCPW.

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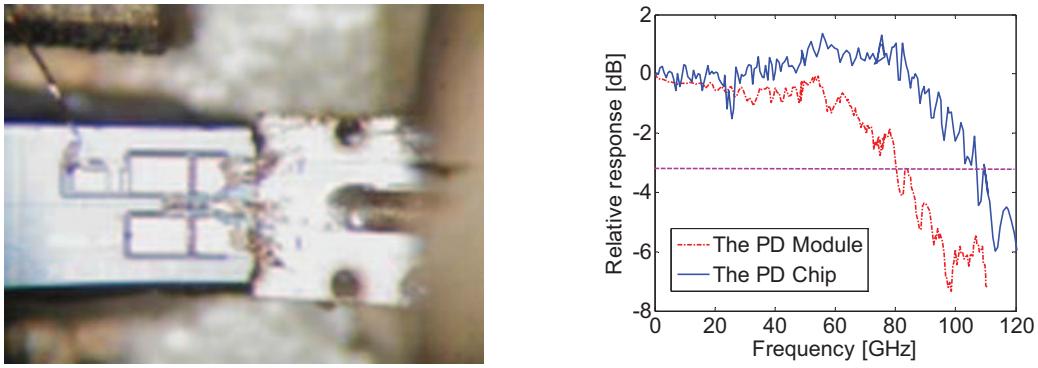
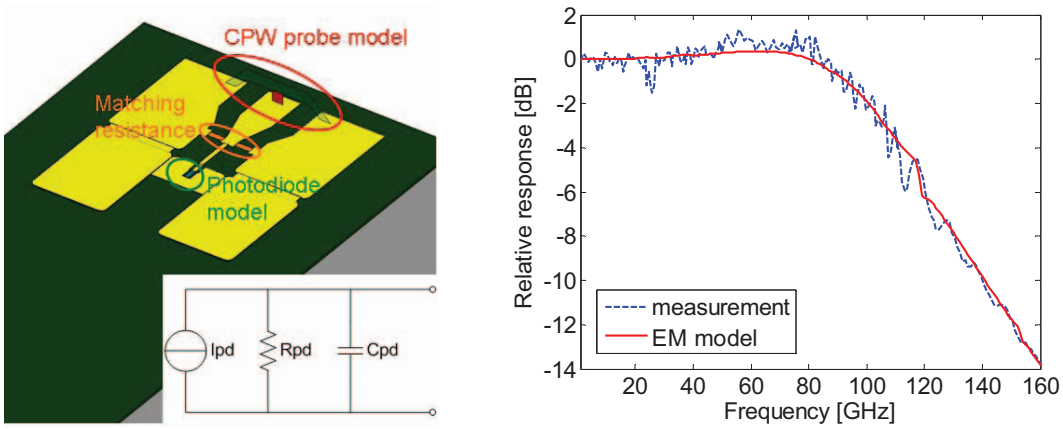
Figures



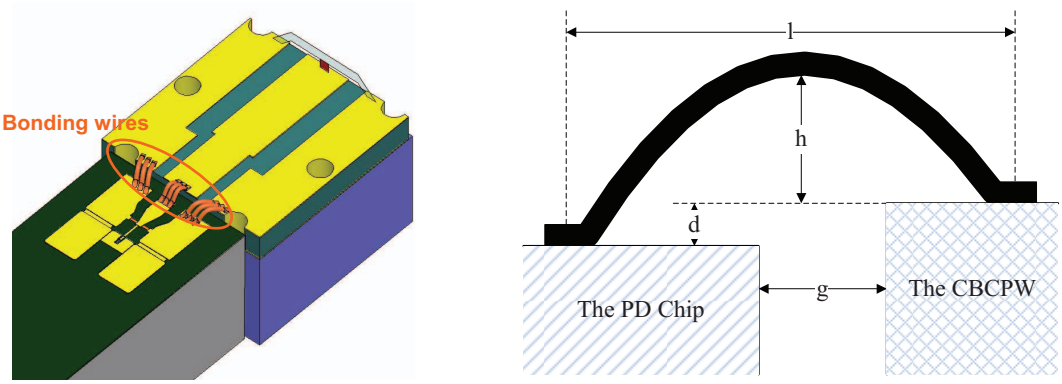
(a) (b)

Figure 1. (a) Microphotograph of the PD module including the packaging structure and the chip; (b) Measured frequency response of the PD module and the chip.



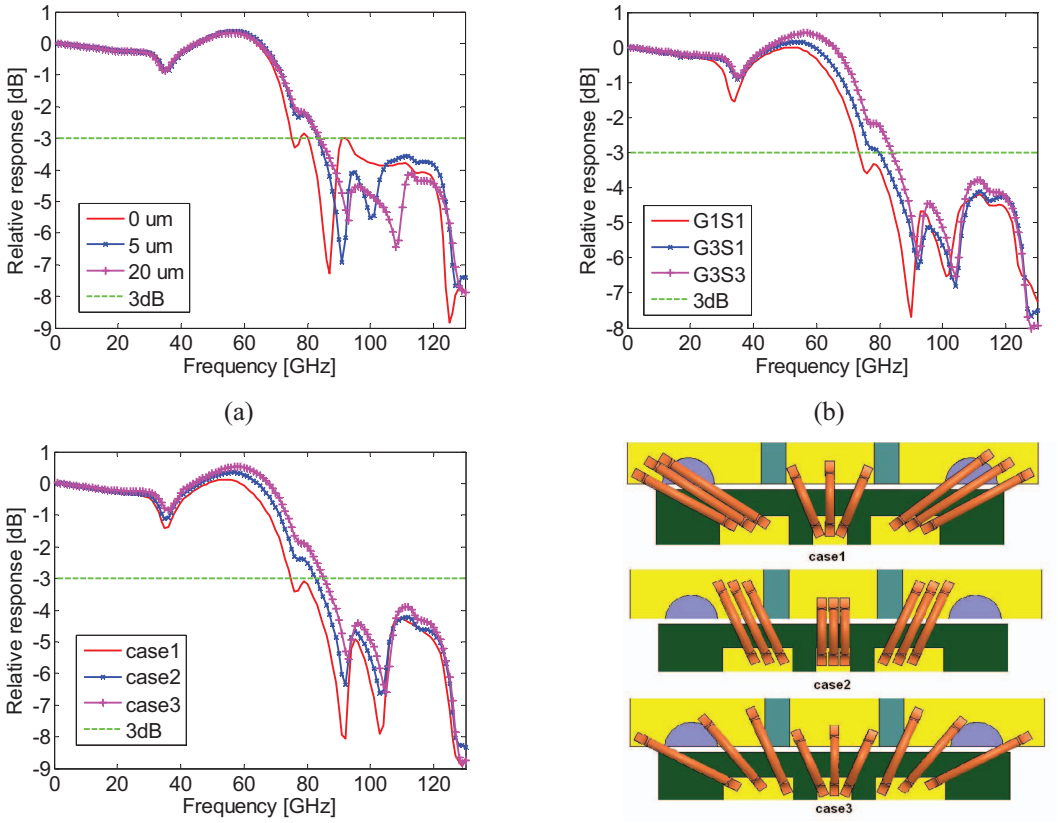
(a) (b)

Figure 2. (a) A fully 3D electromagnetic model of the PD chip, the insert is the equivalent circuit model of the embedded photodiode; (b) Comparison between the measured and the modeled relative response of the PD chip.



(a) (b)

Figure 3. (a) The EM model of the PD chip-to-CBCPW wire-bonding transition; (b) Schematic view of the bonding wires.



(a) (b)

(c) (d)

Figure 4. Simulated relative responses of chip-to-CBCPW wire-bonding transitions; (a) g = 0 μm, 5 μm and 20 μm; (b) different numbers of bonding wires indicated by "GxSy": x and y means the numbers of bonding wires connecting the ground and signal trance, respectively; (c) three typical arrangements of bonding wires as illustrated in (d). g = 20 μm in (b) and (c).

TABLE I

Important Parameters	Negligible Parameters (within certain range)
Gap (g)	Length (l), (S: 60μm~100μm; G: 90μm~150μm)
Number	Height (h), (10μm~50μm)
Arrangement	Horizontal level shifting (d), (-20μm~40μm)*

* Negative value means chips are higher than CBCPWs